IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of — Docket No. p27179

Howard T. Barret

Serial No.: 10/605,109 — Group Art Unit: No. 2825

Filed: September 9, 2003 — Examiner: M. Y. Dimyan

For: **SYSTEM AND METHOD OF AUTOMATICALLY GENERATING KERF DESIGN DATA**

United States Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

REQUEST FOR RECONSIDERATION

UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated December 20, 2005, Applicants request reconsideration in view of the following comments.

A listing of claims is set forth on pages 2-6.

Remarks begin on page 7.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 09-0456.

CLAIMS

A copy of all pending claims and a status of the claims is provided below.

1. (original) A method for generating kerf data, comprising the steps of:
submitting chip data for chip processing;
generating kerf data corresponding to the chip data; and
manipulating the kerf data by use of kerf processing using a same manipulation process as for the chip data.

2. (original) The method of claim 1, wherein the generating step provides for a just-in-time kerf build substantially immediately prior to mask manufacturing.

3. (original) The method of claim 2, wherein the generating step provides for a just-in-time kerf build so that multiple versions of kerf design images are avoided.

4. (original) The method of claim 1, further comprising providing a graphical user interface (GUI) to receive at least one of information and parameters prior to the submitting and generating steps and which is made available to the submitting and generating steps.

5. (original) The method of claim 1, further comprising sharing a same mask order information between the submitting and generating steps.

6. (original) The method of claim 5, wherein the sharing mask order information step includes accessing the mask order information from at least one of a file and a database.

7. (original) The method of claim 1, further comprising the step of manipulating the kerf data and the chip data with substantially a same version of design manipulation software.

8. (original) The method of claim 1, further comprising load balancing at least one of the chip design processing and the kerf processing.

9. (original) The method of claim 1, wherein the manipulating step includes producing kerf test structures for wafer testing.

10. (original) The method of claim 1, wherein in the event an error occurs during at least one of the generating and manipulating step, an email is sent to a destination indicating a nature of the error, such that correction of the error can be made while the chip processing is occurring in order to reduce mean time to repair and to reduce cycle time for the kerf processing.

11. (original) The method of claim 10, further including sending the email if validation checks detect an error in the kerf data, in order to reduce mean time to repair the error.

12. (original) The method of claim 1, wherein at least one of the generating step and the manipulating step occurs concurrently with the chip processing.

13. (original) The method of claim 1, wherein the submitting step produces a chip design image and the manipulating step produces a kerf design image such that the produced chip design image and the kerf design image remain consistent.

14. (original) The method of claim 1, further comprising the steps of:

archiving the manipulated kerf data; and

updating processing logs to record information about at least one of the chip and kerf processing for providing an audit process for debugging issues.

15. (original) A method for generating kerf data, the method comprising the steps of: executing design manipulation utilities for at least chip data design manipulation;

creating a kerf design build utilities file by assembling kerf features previously designed and stored in a library of kerf design data as a result of kerf data manipulation; and

creating and manipulating kerf design data concurrently with chip data design manipulation processing by using same parameters in the kerf design data manipulation and chip data design manipulation thereby ensuring that the kerf design data and the chip design data are consistent.

16. (original) The method of claim 15, wherein in the creating and manipulating step the design data includes one of shrinks, expands and derivation of new data levels.

17. (original) The method of claim 15, wherein in the creating and manipulating step includes processing assist features for device enhancements and addition of nonfunctional shapes for increased manufacturing line process latitude.

18. (original) The method of claim 15, wherein after successful completion of the chip data design manipulation processing, at least one of a chip design image and modified design data is archived in a chip design data repository.

19. (original) The method of claim 15, wherein the creating kerf design data uses information associated with at least one of the chip data and a mask order for the chip, and the information is obtained from a previously created file thereby minimizing user inputs and reducing errors.

20. (original) The method of claim 15, following successful completion of the creating and manipulation step, submitting the kerf design data to validation checks to ensure that the combination of a kerf design grid and a chip design grid prevents grid snapping at the mask write tool.

21. (original) A system for generating kerf data, comprising:

a component to submit chip data for chip processing;

a component to generate kerf data corresponding to the chip data; and

a component to manipulate the kerf data via kerf processing using the same manipulation process as the chip data.

22. (original) The system of claim 21, wherein the component to generate kerf data provides a just-in-time kerf build substantially immediately prior to mask manufacturing and provides a just-in-time kerf build so that multiple versions of kerf design images are avoided.

23. (original) The system of claim 21, further comprising a component to provide a graphical user interface (GUI) to receive at least one of information and parameters which is made available to the component to submit chip data for chip processing and the component to generate kerf data corresponding to the chip data.

24. (original) The system of claim 21, further comprising a means for sharing the same mask order information between all components.

25. (original) The system of claim 21, wherein the chip processing and kerf processing are concurrent, and wherein the chip processing produces a chip design image and the kerf processing produces a kerf design image, the produced chip design image and the kerf design image being consistent.

26. (original) The system of claim 21, further comprising a component to produce kerf test structures for improved reliability of wafer testing.

27. (original) A computer program product comprising a computer usable medium having readable program code embodied in the medium, the computer program product includes:

a first computer program code to submit chip data for chip processing;

a second computer program code to generate kerf data corresponding to the chip data; and

a third computer program code to manipulate the kerf data via kerf processing using the same manipulation process as the chip data.

REMARKS

Claims 1-27 are currently pending in the application. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

Allowed Claims

Applicants appreciate the indication that claims 2, 3 and 20 contain allowable subject matter. However, Applicants submit that all of the claims are in condition for allowance for the following reasons.

35 U.S.C. §102 Rejection

Claims 1, 5-9, 12-19, 21, 22 and 24-27 were rejected under 35 U.S.C. §102(b) for being anticipated by U. S. Patent No. 6,330,708 issued to Parker. This rejection is respectfully traversed.

To reject a claim under 35 U.S.C. §102, a single prior art reference must contain each and every limitation of the claim, either expressly or under the doctrine of inherency. *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Circ), cert. denied, 488 U.S. 892 (1988). In this rejection, the Examiner is of the opinion that the Parker reference includes all of the features of the claimed inventions, and in particular at least the features of each independent claim 1, 21 and 27. Applicants respectfully do not agree wit the Examiner.

By way of example, representative claim 1 recites, in part

> generating kerf data corresponding to the chip data; and
> manipulating the kerf data by use of kerf processing using a same manipulation process as for the chip data.

Claim 15 recites, in part,

> creating a kerf design build utilities file by assembling kerf features previously designed and stored in a library of kerf design data as a result of kerf data manipulation; and
>
> creating and manipulating kerf design data concurrently with chip data design manipulation processing by using same parameters in the kerf design data manipulation and chip data design manipulation thereby ensuring that the kerf design data and the chip design data are consistent.

These features are not shown in the Parker reference.

The Examiner is of the opinion that Parker shows at col. 1, lines 25-38 and col. 3, lines 52-57

> ...manipulating the kerf data by use of kerf processing using the same manipulation process as for the chip.

Applicants do not agree with the Examiner. In Parker, a method is provided for producing CATS, which include files for photomask production. As clearly disclosed in the background section at col. 1, lines 17-25

> The layout for the photomask is created from the pattern files, such as a Moving Electron Beam Exposure (MEBES) data file. <u>The data is based on specific designer inputs which define functional logic and which are subsequently modified for particular semiconductor processes and vendor equipment.</u> The design specification created by the circuit designer is used as an input for algorithms which define photomask structural details. (Emphasis added.)

As should be understood by the above passage, the <u>data for the layout is based on specific designer inputs which are subsequently modified for particular semiconductor processes and vendor equipment.</u> There is simply no disclosure, whatsoever, that the kerf data is manipulated by use of kerf processing using the same manipulation process

as for the chip. In fact, it is not even clear whether the layout information for the photomask, at this stage, includes the kerf data (as discussed in more detail below).

The Examiner is of the opinion that col. 1, lines 25-38 and col. 3, lines 52-57 disclose the step of manipulating the kerf data by use of kerf processing using the same manipulation process as for the chip. However, put into the context of the above passage, col. 1, lines 25-38 merely discloses the use of conventional data conversion and manipulation software. As is described clearly in the background description of the present application, the conventional data conversion and manipulation software includes, for example, submitting kerf data manually and storing in a data library some time prior to the chip design data being sent to the photomask build.

With this in mind, col. 1, lines 25-38 basically mirrors the background section of the present invention. For example, col. 1, lines 25-38 discloses that, using conventional data conversion and manipulation (fracturing) software, the designer's input in the form of levels is subjected to an algorithm which defines the photomask structures. A series of CATS Include Files are created from the results of combining the algorithm with information about the input data, and these Include files are then passed to the CATS execution software which performs the operations and produces the pattern data. Accordingly, col. 1, lines 25-38 does not disclose manipulating the kerf data by use of kerf processing using the same manipulation process as for the chip.

As to col. 3, lines 52-57, this passage discloses that the build information along with algorithms are used to create CATS Include files 24 to produce the MEBES data 31. This passage further discloses that the CATS Include files are instructions for manipulating the various polygon structures present in the design data to define the polygons that will appear on the photomask in a given segment. However, no where in this passage is any teaching, whatsoever, that the kerf is manipulated by use of kerf processing using the same manipulation process as for the chip.

Additionally, it is noted that Parker is directed to formulating an algorithm that may be derived for the Kerf or the product chip. But Parker is not generating kerf data corresponding to the chip data and then manipulating the kerf data by use of kerf processing using a same manipulation process as for the chip data. From a fair reading of Parker, it appears that the Kerf data or steps of the algorithm are constantly be rewritten, under certain circumstances such as discussed at col. 6. However, in view of these passages, it would appear that the generating kerf data is based on the chip data, but there is no suggestion that the kerf data is manipulated by use of kerf processing using a same manipulation process as for the chip data.

Lastly, Parker clearly shows many processing steps at cols. 7-11 for the kerf data. But, it is brought to the Examiner's attention that Parker specifically discloses that these steps apply only to the Kerf structure on the photomask. Parker mentions that a similar process is used to process the actual functional product chip. (col. 11, lines 14-17.) But as disclosed at cols. 11 and 12, the process for the chip is not the same as the Kerf processes. Thus, as seen from the different steps, Parker does not disclose that kerf data is manipulated by use of kerf processing using a same manipulation process as for the chip data. Additionally, Parker does not show creating and manipulating kerf design data is concurrently with chip data design manipulation processing by using same parameters in the kerf design data manipulation and chip data design manipulation to ensure that the kerf design data and the chip design data are consistent.

Claims 5-9, 12-14, 16-19, 22 and 24-27 are dependent claims, depending from respective distinguishable base claims. Accordingly, these claims should also be in condition for allowance, by virtue of their dependencies. Also, Applicants submit that these claims should also be allowable based on their own merits. For example, the applied art does not teach,

1. At least one of the generating step and the manipulating step occurs concurrently with the chip processing (claim 12 and claim 25). Contrary to the Examiner's statement, col. 2, lines 10-48 merely disclose independent creation of algorithms. This does not necessarily mean concurrent.

2. The submitting step produces a chip design image and the manipulating step produces a kerf design image such that the produced chip design image and the kerf design image remain consistent (claim 13).

3. Archiving the manipulated kerf data (claim 14 and claim 18) and updating processing logs to record information about at least one of the chip and kerf processing for providing an audit process for debugging issues (claim 14). Contrary to the Examiner's assertion, there is no teaching that blocks 23, 26, 31, 35 and 35 archive or provide audit processing for debugging.

Accordingly, Applicants respectfully request that the rejection over claims 1, 5-9, 12-19, 21, 22 and 24-27 be withdrawn.

35 U.S.C. §103 Rejection

Claims 4, 10, 11 and 23 were rejected under 35 U.S.C. §103(a) for being unpatentable over Parker in view of "From CIF to Chips". This rejection is respectfully traversed.

Claims 4, 10, 11 and 23 are dependent claims, depending from distinguishable base claims. Accordingly, these claims should also be in condition for allowance, by virtue of their dependencies. Additionally, it is submitted that From CIF to Chips also does not compensate for the deficiencies in Parker and accordingly does not show the features of at least claims 1, 16 and 20.

Accordingly, Applicants respectfully request that the rejection over claims 4, 10, 11 and 23 be withdrawn.

CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,

Andrew M. Calderon
Registration No. 38,093

Greenblum & Bernstein, P.L.C.
1950 Roland Clarke Place
Reston, Virginia 20191
Telephone: 703-716-1191
Facsimile: 703-716-1180